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tree possibilities of the testing: manufacturing level, board level and system level is not shown by the reference to Schwartz. In accordance to the invention the system level tests may be discriminated by the absence of instructions from an external tester. Such selectivity allows more efficiently testing the memory at different stages of manufacturing of board assembly.

Summarizing the above discussion the Applicant highlights the distinguishable features of the present invention which are not shown by the reference to Schwatz:

structurally, the improvement, taught by the present invention, touches the BIST only and thus improves efficiency of chip space usage and allocation; and

the ability to discriminate among three different levels of testing is also unique feature. Further, with reference to claim:

"1. An integrated circuit including an embedded memory and a built-in self-test arrangement including

means for storing test instructions including means for discriminating a source of a test command and receiving test instructions provided from an external tester, ...

means for generating default test instructions, and

means for supplying said default test instructions to said means for storing test instructions "(emphasis added)

It should be noted that all means structures are located within the BIST. Additionally the Examiner asserted in the Office Action that originally filed claims do not explicitly differentiate among three possibility of testing. This is incorrect, because the original method claim 17 states in the preamble that a BIST discriminate among manufacturing and board level testing. In order to highlight this feature claims 1, 8 were amended by this amendment.

Responding to the Examiner statement that "test command" in the present invention and debug signal in Schwartz are analogous. Applicant respectfully submits that the principal of initiating of the testing claimed in the present invention is different. The present invention discriminates of a source of a test command for performing manufacturing level and board level testing, in addition the system level test performed in absence of any signal. In contrast, in Schwartz testing is always initiated by debagging signal and no different levels of testing is

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distinguished.

In view of the foregoing amendments and remarks, Applicant submits that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicant hereby makes a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041 (Whitham, Curtis & Christofferson, P.C.).

Respectfully submitted,

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Comparison chart of the present invention and primary reference to Schwarz

	Claimed Invention	Schwarz
Field of Technology	programmable memory BIST arrangement	reconfigurable built-in self test circuit for the debugging an embedded device
Problem Solved	Providing a testing of storage cells at different stages of manufacturing and operation.(manufacturing level, operation level and system level)	Customizing the BIST circuitry to provide assistance in determining the cause of detected failure without complexity added to the integrated circuit.
Structure	BIST additionally has means for storing test instruction, means for discriminating a source of a test command for performing manufacturing level and board level testing, means for receiving test instructions provided from external tester, means for generating default test instructions, means for supplying default test instruction to meas for string test instructions.	BIST circuitry includes a two multiplesxers, buffer and comparator which help to BIST be modifyed.
Function	Significant reduction of a ration of the maximum extent of the housing to the length of the middle section of the light emitting tube.	Proving a testing from BIST or from external tester increasing a flexibility of BIST usage.
Advantages	1. Providing an ability of testing in different stages of manufacturing and operation. 2.Improves efficiency of chip space usage and allocation.	Providing an effective debugging by proving an ability of modifying the test.